WHAT IS CLAIMED IS:

1. A memory module buffer comprising:

a host-side memory channel port and a memory device channel port;

a command decoder to decode commands received at the host-side memory channel port, the commands including at least one implicit command type; and

a memory device access controller to respond to a command having an implicit command type by generating at least one explicit memory access command to the memory device channel port.

2. The memory module buffer of claim 1, wherein the at least one implicit command type includes at least one implicit write command with a command format that specifies a first region of memory to be written to and includes less explicit write data than would be needed to fill the region of memory, the buffer further comprising a write data generator to form implicit write data in accordance with the implicit write command.

3. The memory module buffer of claim 2, wherein the at least one implicit write command includes a copy command specifying a second region of memory to be read from to form the implicit write data, the memory device access controller responding to the copy command by causing the buffer to read data from the second region of memory to form the implicit write data.

4. The memory module buffer of claim 3, wherein when the second region of memory is smaller in size than the first region of memory, the write data generator forms implicit write data by repeating at least some data from the second region of memory.

5. The memory module buffer of claim 2, wherein the at least one implicit write command includes a command comprising a data value, and wherein the write data generator forms implicit write data by repeating the data value for multiple addresses throughout the first region of memory.

6. The memory module buffer of claim 2, wherein the at least one implicit write command includes a command indicating that a predefined pattern is to be written to the first region of memory, and wherein the write data generator forms implicit write data by repetitively generating the predefined pattern.

7. The memory module buffer of claim 6, further comprising a pattern register coupled to the write data generator to store the predefined pattern.

8. The memory module buffer of claim 6, wherein the predefined pattern is at least partially dependent on the address being written to, and wherein the write data generator forms implicit write data using at least a portion of the address being written to.

9. The memory module buffer of claim 2, wherein the at least one implicit write command includes a command having a format capable of specifying the first region of memory as a non-contiguous region of multiple disconnected sub regions, the memory device access controller having the capability to direct writing to each of the multiple disconnected sub regions in turn.

10. The memory module buffer of claim 9, the memory device access controller having the capability to respond to a command format specifying a start address, write length, skip

length, and number of sub regions, by repetitively writing data to a range of addresses equal to the write length and skipping a range of addresses equal to the skip length, until a number of sub regions equal to the specified number of sub regions has been written.

11. The memory module buffer of claim 2, wherein the write data generator comprises an error correction code generator capable of generating an error correction code as part of an implicit write data word.

12. The memory module buffer of claim 2, the memory device channel port having a data width, the buffer further comprising a data mask generator to mask a portion of the data width during writes responsive to an implicit command type when an implicit command specifies a partial-width write command.

13. The memory module buffer of claim 1, further comprising a pause function activated by the command decoder when a second command requiring access to the memory device channel port is received during activity related to a first command of an implicit command type, the memory device access controller responding to the pause function by pausing execution of the first command while the second command executes.

14. The memory module buffer of claim 1, further comprising a completion register that the memory module buffer sets to indicate the status of a pending command with an implicit command type, wherein the value stored in the completion register is accessible from the host-side memory channel port.

15. The memory module buffer of claim 1, the memory device access controller having the

capability to respond to a command format specifying a start address, read length, skip length, and number of sub regions, by repetitively reading data from a range of addresses equal to the read length and skipping a range of addresses equal to the skip length, until a number of sub regions equal to the specified number of sub regions has been read.

16. A method of writing data to memory on a buffered memory module, the method comprising:

receiving, at a buffer on the module, a command specifying an implicit write to the memory;

in response to the implicit command, forming at least one first data word/first write address combination for an explicit write to the memory; and

transmitting the data word and write address to the memory as part of a first explicit write command.

17. The method of claim 16, further comprising:

reading a stored data word from the memory in response to the implicit command; and

forming the at least one data word using the stored data word.

18. The method of claim 17, wherein reading a stored data word from the memory and forming the at least one data word using the stored data word are repeated for multiple memory locations in response to the implicit command.

19. The method of claim 16, wherein forming at least one data word/write address combination for an explicit write to the memory comprises repeating a data value specified by the implicit command for multiple write addresses.

20. The method of claim 19, wherein the data value specified by the implicit command is determined by reading a value from a pattern register.

21. The method of claim 16, wherein forming at least one data word/write address combination comprises forming a data word that at least partially depends on the write address.

22. The method of claim 16, wherein the command specifies multiple non-contiguous sub-regions of memory, the method further comprising transmitting a second data word and second write address to the memory as part of a second explicit write command, the second write address non-contiguous with the first write address.

23. The method of claim 16, wherein forming at least one first data word comprises generating an error correction code to be written with the data word.

24. A buffered memory module comprising:

a plurality of memory devices; and

a buffer connected to the memory devices and having

a host-side memory channel port,

a command decoder to decode commands received at the host-side memory channel port, the commands including at least one implicit command type, and

a memory device access controller to respond to a command having an implicit command type by generating and transmitting at least one explicit memory access command to the memory devices.

25. The buffered memory module of claim 24, wherein the at least one implicit command type includes at least one implicit write command with a command format that specifies a first region of memory to be written to and includes less explicit write data than would be needed to fill the region of memory, the buffer further comprising a write data generator to form implicit write data in accordance with the implicit write command.

26. The buffered memory module of claim 24, the memory device access controller having the capability to respond to a command format specifying a start address, read length, skip length, and number of sub regions, by repetitively reading data from a range of addresses equal to the read length and skipping a range of addresses equal to the skip length, until a number of sub regions equal to the specified number of sub regions has been read from the memory devices.

27. An article of manufacture comprising computer-readable media containing instructions that, when executed by a processor, cause that processor to perform a method comprising:

forming an implicit memory command; and

transmitting the implicit memory command to a buffered memory module for expansion to one or more explicit memory commands.

28. The article of manufacture of claim 27, wherein the implicit memory command specifies a start address, read length, skip length, and number of sub regions to read, the method further comprising processing a block of read data returned by the buffered memory module with knowledge of the read and skip length.

29. The article of manufacture of claim 27, wherein the implicit memory command specifies a write command and indicates how the buffered memory module is to construct write data and/or write addresses for multiple write cycles.

30. A computing device comprising:

a processor;

a first buffered memory module comprising a plurality of memory devices and a buffer connected to the memory devices, the buffer having

a host-side memory channel port,

a command decoder to decode commands received at the host-side memory channel port, the commands including at least one implicit command type, and

a memory device access controller to respond to a command having an implicit command type by generating and transmitting at least one explicit memory access command to the memory devices; and

a first point-to-point memory channel coupling the processor to the buffered memory module.

31. The computing device of claim 30, wherein the buffer on the first buffered memory module further comprises a downstream memory channel port, the computing device further comprising:

a second buffered memory module having a host-side memory channel port; and

a second point-to-point memory channel connecting the first buffered memory module downstream memory channel port to the second buffered memory module host-side memory channel port;

the computing device having the capability to issue an implicit command to the first

memory module and issue another command through the first memory module to the second memory module while the first memory module is executing explicit commands in response to the implicit command.